Amendments to the Claims

1. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

an oxide layer formed on said semiconductor layer, said oxide layer having a substantially uniform thickness;

a gate structure formed on a portion of said oxide layer and having first and second leading edges; and

a first overlap region of the oxide layer located only beneath said gate structure and adjacent said first leading edge and inward of said second leading edge and a second overlap region of the oxide layer located only beneath said gate structure and adjacent said first overlap region and said second leading edge, said first overlap region having a predetermined ion implant concentration higher than in said second overlap region and all remaining oxide layer portions extending outwardly from both said first and second leading edges of said gate structure, said predetermined implant concentration being sufficient to increase the electrical gate oxide thickness in said overlap region.

2. (Original) The circuit structure according to claim 1, wherein said predetermined ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

3. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

a source region and a drain region in said semiconductor layer which are lightly doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region, said gate oxide layer having a substantially uniform thickness; and

a gate electrode located on a portion of said gate oxide layer, wherein said portion of said gate oxide layer includes a first overlap region which is only beneath said gate electrode inward of said source region and adjacent said drain region and a second overlap region which is only beneath said gate electrode and adjacent said first overlap region and said source region, said first overlap region having an ion implant concentration higher than in said second overlap region and all remaining portions of said oxide layer extending outwardly from both sides of the gate electrode, which is effective to lower the surface electrical field in said overlap region.

4. (Original) The circuit structure according to claim 3, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

5. (Original) The circuit structure according to claim 3, wherein said source region and said drain region are heavily doped with a second conductivity dopant.

6. (Previously presented) The circuit structure according to claim 3, further including a pair of spacers adjacent said gate electrode.

7. (Original) The circuit structure according to claim 3, wherein said gate electrode is comprised of polysilicon.

8. (Original) The circuit structure according to claim 3, wherein said gate electrode is a gate stack.

9. (Original) The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

10. (Previously presented) The circuit structure according to claim 3, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium nitride layer.

11. (Previously presented) The circuit structure according to claim 3, further including a pair of conductive studs and an interlevel dielectric layer provided on said semiconductive layer, said interlevel dielectric layer have a pair of through-holes, each accommodating one of each said pair of conductive studs, and one of each said pair of conductive studs contacting one of each said source/drain regions.

12. (Currently Amended) A circuit structure comprising:

a semiconductor layer;

a first dopant-type MOS transistor is situated on said semiconductor layer having:

a source region and a drain region in said semiconductor layer which are doped with a first conductivity-type dopant;

a channel region located between said source/drain regions;

a gate oxide layer located on a surface of said channel region, said gate oxide layer having a substantially uniform thickness; ~~and~~

a gate electrode located on a portion of said gate oxide layer, wherein the portion of said gate oxide layer includes a first overlap region which is only beneath said gate electrode inward of said source region and adjacent said drain region and a second overlap region which is only beneath said gate electrode and adjacent said first overlap region and said source region, said first overlap region having an ion implant concentration higher than in said second overlap region and all remaining portions of said gate oxide layer extending outwardly from both sides of the gate electrode, which is effective to lower the surface electrical field in said overlap region; and,

a second-type dopant MOS transistor which is complementary to said first dopant-type MOS transistor, said second-type dopant MOS transistor is situated on said semiconductor layer and includes a second gate oxide layer, two complementary source/drain regions which are doped with a second conductivity-type dopant, and a complementary gate electrode located on said second gate oxide layer.

13. (Original) The circuit structure according to claim 12, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

14. (Previously presented) The circuit structure according to claim 12, wherein a portion of said second gate oxide layer which is beneath said complimentary gate electrode and adjacent said complimentary drain region, and which defines a second overlap region, having an ion implant concentration which is effective to lower the surface electrical field in said second overlap region.

Claims 15-44 (Canceled).

45. (Currently Amended) A circuit structure comprising:

a semiconductor layer having a source region, a drain region, and a channel region located between said source/drain regions;

a gate oxide layer located at least on a surface of said channel region, said gate oxide layer having a substantially uniform thickness; and

a gate electrode located on a portion of said gate oxide layer, wherein the portion of said gate oxide layer only beneath said gate electrode has first and second portions, and said first portion has a higher ion implant concentration than in said second portion and all remaining portions of said gate oxide layer extending outwardly from both sides of said gate electrode.

46. (Previously Presented) The circuit structure according to claim 45, wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

47. (Currently Amended) A circuit structure comprising:

a semiconductor layer having a pair of field isolation regions and a channel region, said channel region is located between said pair of field isolation regions;

a gate oxide layer located at least on a surface of said channel region, said gate oxide layer having a substantially uniform thickness; and

a gate electrode located on said gate oxide layer, said gate oxide layer only beneath said gate electrode having a first portion and a second portion, said first portion having a higher ion implant concentration than in said second portion and all remaining portions of said gate oxide layer between said pair of field isolation regions.

48. (Previously Presented) The circuit structure according to claim 47 wherein said ion implant concentration is about 1E18 atoms per cubic centimeter of fluorine.

49. (Previously Presented) The circuit structure according to claim 47 wherein said semiconductor layer further comprises a source region and a drain region, and said first portion is adjacent said drain region.

50. (Previously Presented) The circuit structure according to claim 47, further comprising a pair of spacers adjacent said gate electrode.

51. (Previously Presented) The circuit structure according to claim 47, wherein said gate electrode is comprised of polysilicon.

52. (Previously Presented) The circuit structure according to claim 47, wherein said gate electrode is a gate stack.

53. (Previously Presented) The circuit structure according to claim 47, wherein said gate electrode is comprised of a layer of polysilicon, and one or more additional layers selected from the group consisting of metals, metal alloys, highly doped polysilicon, silicides, and polycides (polysilicon/metal silicide stacks).

54. (Previously Presented) The circuit structure according to claim 47, wherein said gate electrode is comprised of a layer of polysilicon, a layer of titanium nitride deposited on said polysilicon layer, and a layer of tungsten deposited on said titanium nitride layer.

55. (Previously Presented) The circuit structure according to claim 47, wherein said oxide layer extends between said pair of field isolation regions.

56. (Previously presented) The circuit structure according to claim 3, wherein said source region and said drain region each have a first dopant and a second dopant, said second dopant extending deeper into said semiconductor layer than said first dopant.

57. (Previously presented) The circuit structure according to claim 47, further comprising an interlevel dielectric layer provided on said semiconductive layer, said interlevel dielectric layer having a through-hole accommodating a conductive stud, wherein said semiconductor layer further comprises a drain region adjacent said first portion, and wherein said conductive stud contacts said drain region.